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# A 0.7 V 0.0017 mV/V CMOS Voltage Reference with No Amplifier

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## Abstract:

A low-supply voltage, high-power supply rejection ratio (PSRR), low-line sensitivity (LS) CMOS voltage reference with no amplifier is presented in this paper. The low LS is realized by the supply voltage independent bias currents. The circuit only consists of CMOS transistors and a resistor, which will decrease the supply voltage and area. The proposed voltage reference is designed in the standard 0.18 μm CMOS process. The simulation results show that the minimum power supply voltage is lower than 0.7 V. The temperature coefficient (TC) is 50 ppm/℃ to 56 ppm/℃ for a wide temperature range of -40℃ to 130℃, while the power consumption is 4.35 μW at 0.7 V. The simulated line sensitivity is 0.0017 mV/V at room temperature. Under the TT process corner, the simulated PSRR is -91.5 dB at 1 KHz when the supply voltage is 0.7 V.

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## I. INTRODUCTION

As an essential building component in integrated circuits, voltage reference is widely used in A/D and D/A converters, phase locked loops [1] and so on. With the development of low power applications such as portable devices and wireless sensor networks [2, 3], low-voltage circuits have attracted considerable attention.

Voltagereferences[4-6] are implemented through Bipolar Junction Transistors (BJTs). However, since the turn-on voltage of the BJT is typically 0.7 V, a high power supply voltage is required. This does not meet the requirements of modern low voltage and low power consumption. In order to work out the problem, Yang *et al.* [7] exploit supply voltage boost to reduce power supply voltage, but charge-pump and digital control circuits increase the area and the power consumption.

There are no BJTs or boost circuits in [8-10], which use MOSFET-only to achieve low voltage and low power consumption. However, the current of the biasing circuits is so sensitive to the power supply voltage that it produces a very poor line sensitivity (LS). Meanwhile, the junction leakage current may seriously affect the subthreshold characteristics of the MOSFETs[11], resulting in most nanowattsubthreshold voltage references only operate reliably over a limited temperature range. Therefore, high power consumption is required to obtain a wide temperature range and a low temperature coefficient (TC).

LS directly affects the power supply rejection ratio (PSRR) of the circuits, so it should be as small as possible [12]. To achieve a low LS voltage reference, amplifier is utilized in [13, 14] to increase the loop gain on the bias circuit. However, the amplifier consumes the voltage headroom. another method employs cascode stages [15], which increases the minimum supply voltage.

In this paper, in order to improve LS, we use negative feedback technique to obtain a current source which is independent of the voltage source.Through body-bias technique, a low TC voltage can be achieved.

## II. PRINCIPLE OF THE PROPOSED VOLTAGE REFERENCE

The principle of the voltage reference is shown in Fig. 1[9]. The voltage reference consists of current sources and three NMOS transistors operating in the subthreshold region. In such structure, when the MOSFET works in the sub-threshold region, the drain current $I_D$ of the MOSFET is given by [12]

$$I_D = \mu C_{ox}(\eta-1)\left(\frac{W}{L}\right)V_T^2 \exp^{\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)}\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \quad (1)$$

where $\mu$ is the carrier mobility, $C_{ox}$ is the gate-oxide capacitance, $\eta$ is the sub-threshold slope factor, $W/L$ is the transistor aspect ratio, $V_T = K_BT/q$ is the thermal voltage, $K_B$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the elementary charge, and $V_{TH}$ is the threshold voltage of the MOSFET, $V_{GS}$ and $V_{DS}$ are the gate-source voltage and drain-source voltage of the MOSFET, respectively. For $V_{DS} \geq 4V_T$, the current $I_D$ is independent of $V_{DS}$,thus the gate-source voltage of M3 can be approximated by

$$V_{GS,M3} = V_{TH,M3} + \eta V_T \ln\left[\frac{I}{\mu C_{ox}(\eta-1)\left(\frac{W}{L}\right)_{M3}V_T^2}\right]. \quad (2)$$

Since there is a body effect in M1, the threshold voltage of M1 can be expressed as [16, 17]

$$\begin{aligned} V_{TH} &= V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) \\ &\approx V_{TH0} + (\eta-1)V_{SB} \end{aligned} \quad (3)$$

where $V_{TH0}$ is the threshold voltage with zero body bias, $\gamma$ is the body effect constant, $\Phi_F$ is the Fermi potential and $V_{SB}$ is the source-bulk voltage of M1.

Then, using (2) and (3), reference voltage $V_{REF}$ can be acquired as

$$\begin{aligned} V_{REF} &= V_{GS,M2} - V_{GS,M1} \\ &= \gamma\left(\sqrt{2\phi_F} - \sqrt{2\phi_F + V_{REF} - V_{GS,M3}}\right) + \eta V_T \ln\frac{K_{M1}}{K_{M2}} \end{aligned} \quad (4)$$

where $K_{M1}$ and $K_{M2}$ are the aspect ratios of M1 and M2, respectively.

Furthermore, (4) can be rearranged as

$$V_{REF} = \Delta V'_{GS} + f\left(V_{GS,M3}\right) \quad (5)$$

where $\Delta V'_{GS} = \eta V_T \ln\left(K_{M1}/K_{M2}\right)$,

$$f\left(V_{GS,M3}\right) = \left(\gamma\left(\gamma + 2\sqrt{2\phi_F}\right)/2\right) - \gamma\sqrt{\gamma\left((\gamma/4) + \sqrt{2\phi_F}\right) + 2\phi_F + \eta V_T \ln\left(K_{M1}/K_{M2}\right) - V_{GS,M3}}.$$

In view of the fact that the current source $I$ is related to $V_{DD}$, we have

$$\begin{aligned} \frac{\partial V_{GS,M3}}{\partial V_{DD}} &= \eta V_T \frac{\mu_n C_{ox}(\eta-1)K_{M3}V_T^2}{I}\frac{\partial I}{\partial V_{DD}} \\ &\quad \times \frac{1}{\mu_n C_{ox}(\eta-1)K_{M3}V_T^2} \\ &= \frac{\eta V_T}{I}\frac{\partial I}{\partial V_{DD}}. \end{aligned} \quad (6)$$

The PSRR can be evaluated by taking the derivative of (5) with respect to $V_{DD}$ and inserting (6)

$$\begin{aligned} \frac{\partial V_{REF}}{\partial V_{DD}} &= -\gamma \frac{-\frac{\partial V_{GS,M3}}{\partial V_{DD}}}{2\sqrt{\gamma\left(\frac{\gamma}{4} + \sqrt{2\phi_F}\right) + 2\phi_F + \eta V_T \ln\frac{K_{M1}}{K_{M2}} - V_{GS,M3}}} \\ &= \frac{\gamma}{I}\frac{\eta V_T \frac{\partial I}{\partial V_{DD}}}{2\sqrt{\gamma\left(\frac{\gamma}{4} + \sqrt{2\phi_F}\right) + 2\phi_F + \eta V_T \ln\frac{K_{M1}}{K_{M2}} - V_{GS,M3}}}. \end{aligned} \quad (7)$$

From (7), we can find that the PSRR of the circuit mainly depends on the variation of $I$ with $V_{DD}$. Therefore, in order to achieve high PSRR and low LS, a current source that is independent of the power supply should be considered.

[18] utilizes the difference in gate-source voltage of MOS transistors across the resistor $R$ to obtain the bias current. Unfortunately, the variation of the current with the power supply voltage is relatively large due to the channel length modulation effects. In [9], a resistor-less bulk-driven current generator circuit is proposed. The bulk-driven MOS transistor is operated as a resistor in the deep triode region, which canachieve a nano-ampere current without increasing the chip area. However, since the MOS transistors operating in the subthreshold region have an asymmetric bias configuration,

the circuit is very sensitive to the supply voltage variations. So all of these current generators result in poor LS.

To obtain a current generator which is independent of$V_{DD}$, we use negative feedback technique [19] without amplifier and cascade stages.

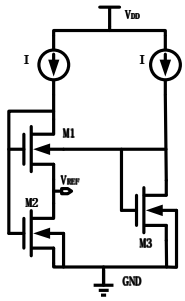


Fig. 1Principle of the voltage reference

The schematic of the proposed voltage reference is illustrated in Fig.2. The circuit consists of start-up circuit, current generator, output stage and body bias circuit. The start-up circuit helps the circuit get rid of the degeneracy point and enter the second steady state. TheMOSFETs MP1-MP5are operated in the saturation region, and MN1-MN5 work in the subthreshold region. Main section will be described in the following.

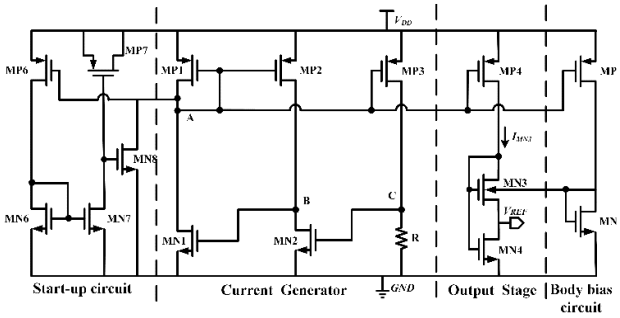


Fig. 2Schematic of the proposed voltage reference

### *A. Current Generator*

In the current generator, the negative feedback loop is composed of MN2, MN1, MP1, and MP3. Therefore, when the node voltage C rises with the power supply variation, the voltage of the node B drops, and then the node A rises. Since the negative feedback is greater than the positive feedback formed by MN1, MP1, MP2, the node C falls at last, and vice versa. In this way, it is guaranteed that the current flowing through the resistor $R$ remains constant.

From Fig. 2. $V_{GS,MN2}$is the voltage across$R$.The current flowing through $R$ can be described as $I_R = V_{GS,MN2}/R$. Due to $(W/L)_{MP1} = (W/L)_{MP2} = (W/L)_{MP3}$, we can get that the current flowing through $R$ is approximately equal to the currents of transistor MN2 and MN1. The temperature dependence of threshold voltage can be expressed as [10]

$$V_{TH} = V_{TH0} - \delta\left(T - T_0\right) \quad (8)$$

where$T_0$ is the reference temperature, $\delta$ is the threshold temperature exponent. The nonlinear temperature dependence of mobility is $\mu(T) = \mu(T_0)(T/T_0)^{-\alpha}$, where $\mu(T_0)$ is the carrier mobility at temperature $T_0$, $\alpha$ is the mobility temperature exponent about 1.5-2 [20].

Since $V_{GS}$ decreases with temperature for any fixed drain current $I_D$, we can approximate write as [21]

$$V_{GS} = V_{GS0} - \beta\left(T - T_0\right) \quad (9)$$

where$\beta$ is positive quantity, $V_{GS0}$ is the gate-source voltage at the temperature $T_0$.

Therefore, for $V_{DS} \geq 4V_T$, substituting the expressions (8) and (9) into (1), the expression of current flowing through MN2 can be got

$$I_{D,MN2} = \mu(T_0)T_0^2 C_{ox}\left(\eta - 1\right)\left(\frac{W}{L}\right)_{MN2}\frac{K_B^{\,2}}{q^2}\cdot \exp\left(\frac{(\delta-\beta)q}{\eta K_B}\right)\cdot\exp\left(\frac{m}{\eta T}\right). \quad (10)$$

Here, m = $V_{GS0}$-$V_{TH0}$+$T_0$ ($\beta$-$\delta$) is a constant. When MN1 and MN2 are operated in the subthreshold region to reduce the minimum supply voltage. MP1-MP3 work in the saturation region to help reduce current mismatch. In addition, the negative feedback loop also ensures the constancy of the current when the supply voltage changes, the principle of which will be discussed below.

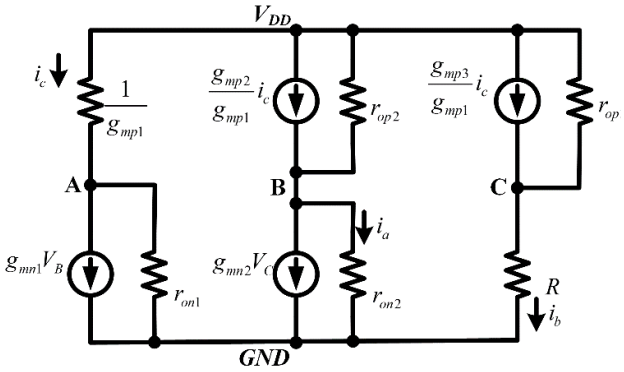


Fig. 3Small-signal equivalent model of the current generator

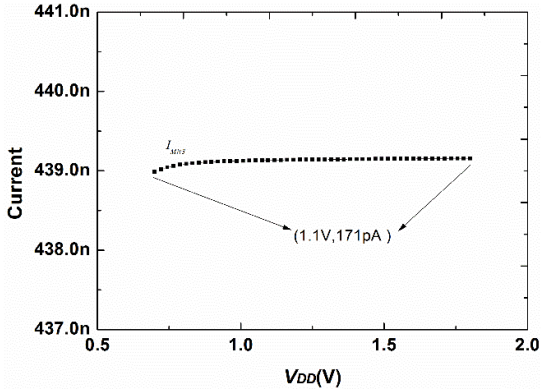


Fig. 4 Simulated current of IMN3 versus supply voltage

Fig. 3 shows the small signal model of the current generator. From Fig. 3, we can get the following expression according to Kirchhoff's current law

$$i_c = g_{mp1}\left(V_{DD} - V_A\right) = g_{mn1}V_B + \frac{V_A}{r_{on1}}, \quad (11)$$

$$i_a = \frac{g_{mp2}}{g_{mp1}} i_c + \frac{V_{DD} - V_B}{r_{op2}} - g_{mn2}V_C = \frac{V_B}{r_{on2}}, \quad (12)$$

$$i_b = \frac{g_{mp3}}{g_{mp1}} i_c + \frac{V_{DD} - V_C}{r_{op3}} = \frac{V_C}{R}. \quad (13)$$

Through simultaneous equations (11)-(13), the relationship between $i_c$ and $V_{DD}$ can be expressed as

$$\frac{i_c}{V_{DD}} \approx \frac{g_{mp1}g_{mn1}r_{op3} - g_{mp1}g_{mn1}r_{op2}g_{mn2}R}{\frac{(R + r_{op3})r_{op2}g_{mp1}}{r_{op2}//r_{on2}} + g_{mn1}r_{op2}(g_{mn2}g_{mp3}r_{op3}R - g_{mp2}(R + r_{op3}))}. \quad (14)$$

where$g_{mni}$ represents the transconductance of MNi, $g_{mpi}$ represents the transconductance of MPi, $r_{oni}$ represents the output resistance of MNi, $r_{opi}$represents the output resistance of MPi. From Expression (14), it is obvious that the sensitivity of $i_c$ to $V_{DD}$ is proportional to $R$ and $g_{mn2}$. Consequently, the sizes of the resistor $R$ and the transistor MN2 are appropriately adjusted to obtain a current source independent of $V_{DD}$. The current of the current generator is mirrored to the output stage through transistor MP4. As shown in Fig. 4, the current $I_{MN3}$ of the output stage changes only 171 pAwhen the supply voltage changes 1.1 V.

### *B. Output Stage*

The output stage circuit is formed by MN3 and MN4 operating in the subthreshold region. With the body-bias technique, the threshold voltages of MN3 and MN4 are different. In this way, a low TC $V_{REF}$ is obtained. Since the source-bulk voltage of MN3 is not zero, the body effect exists. Therefore, using the same derivation method used in expression (6) in Section 2, reference voltage $V_{REF}$becomes

$$V_{REF} = \Delta V'_{GS} + f\left(V_{GS,MN5}\right) \quad (15)$$

where $\Delta V'_{GS} = \eta V_T \ln\left(K_{MN3}/K_{MN4}\right)$,

$$f\left(V_{GS,MN5}\right) = \left(\gamma\left(\gamma + 2\sqrt{2\phi_F}\right)\Big/2\right) - \gamma\sqrt{\gamma\left((\gamma/4) + \sqrt{2\phi_F}\right) + 2\phi_F + \eta V_T \ln\left(K_{MN3}/K_{MN4}\right) - V_{GS,MN5}},$$

$$V_{GS,MN5} = V_{TH,MN5} + \eta V_T \ln\frac{bI_{D,MN2}}{\mu(T_0)C_{ox}(\eta - 1)K_{MN5}V_T^2}$$

$$= \eta V_T \ln\frac{bK_{MN2}}{K_{MN5}} + (\delta - \beta)T + V_{GS0} - V_{TH0} + T_0(\beta - \delta) + V_{TH,MN5}$$

where b=$K_{MP5}/K_{MP2}$, and $K_{MP2}$, $K_{MN3}$, $K_{MN4}$, $K_{MN5}$, $K_{MP5}$ are the aspect ratios of MP2, MN3, MN4, MN5, and MP5, respectively. $\Delta V'_{GS}$ is the gate-source voltage difference between MN3 and MN4 when the substrate of MN3 is connected to ground and has a positive TC. $V_{GS,MN5}$ and f($V_{GS,MN5}$) are a negative TC voltage because the slope of $V_{TH,MN5}$ is larger than that of $V_T$. The two opposite TC voltages ($\Delta V'_{GS}$, f($V_{GS,M25}$)) are combined together to generate a temperature-independent $V_{REF}$.

By Simplifying (15), the output voltage $V_{REF}$ can be got as

$$V_{REF} = A + BT - \gamma\sqrt{C + BT - DT - E} \quad (16)$$

where $A = \left(\gamma\left(\gamma + 2\sqrt{2\phi_F}\right)/2\right)$, $B = \eta\frac{K_B}{q}\ln\left(\frac{K_{MN3}}{K_{MN4}}\right)$,

$C = \gamma\left((\gamma/4) + \sqrt{2\phi_F}\right) + 2\phi_F$, $D = \eta\frac{K_B}{q}\ln\frac{K_{MP5}K_{MN2}}{K_{MP2}K_{MN5}} - \beta$,

$E = \beta T_0 + V_{GS0,MN2}$.

According to (16), the first derivative of $V_{REF}$ with temperature can be expressed as

$$\frac{\partial V_{REF}}{\partial T} = B - \gamma\frac{B - D}{2\sqrt{C + (B - D)T - E}}. \quad (17)$$

Let $\partial V_{REF}/\partial T = 0$, we can get

$$T = \frac{\gamma^2 (B - D)}{4B^2} + \frac{E - C}{B - D}. \quad (18)$$

By adjusting the $K_{MN3}$-$K_{MN5}$ properly, we can get a low TC voltage reference over a wide temperature range.

## III. SIMULATION RESULTS

Based on TSMC 0.18 µm CMOS process, the pre-simulations and post layout simulations of proposed voltage reference have been finished. Fig. 5 shows the layout of the proposed voltage reference. The total layout area is 0.0067 mm$^2$.

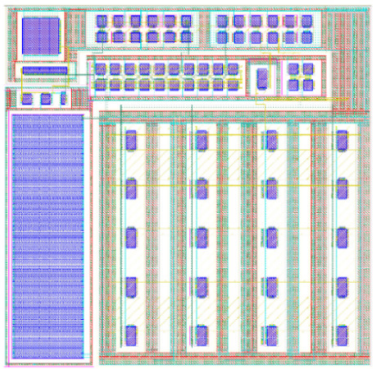

Fig. 5 Layout of proposed voltage reference

Fig. 6 shows the simulation results of the reference voltage versus temperature in the range of -40℃ to 130℃ at different process corners. It is worth noting that the reference voltage has the same trend with temperature at different process corners. As described in Section 2, a low TC is achieved. We can get that the best TC is 50 ppm/℃ at FS process corner, and the worst TC is 56 ppm/℃ at SS process corner. The inset of Fig. 6 is the comparing between the pre-simulation and the post-simulation at the TT process corner, we can find that the difference between the pre-simulation and post simulation results is very small, so the design of circuit is reasonable.

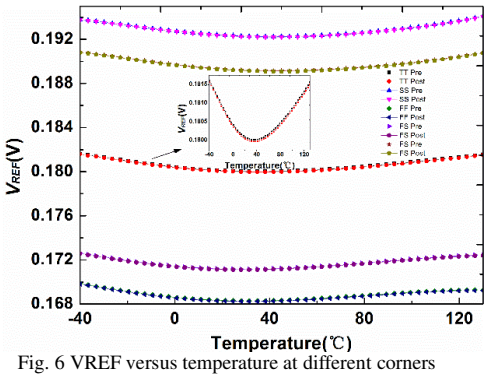


Fig. 6 VREF versus temperature at different corners

Fig. 7 shows the simulated PSRR at different process corners when $V_{DD}$ is 0.7 V. The highest PSRR is -101.5 dB at 1 KHz when process corner is FF. The worst PSRR is -82.6 dB at 1 KHz when process corner is SS. As mentioned earlier, through the negative feedback technique, the variation of current source with power supply voltage is very small (see Fig. 4). Therefore, Fig. 7 shows the result of (7), we can find that a high PSRR is obtained at different process corners. The inset of Fig. 7 shows the PSRR at FS Pre and FF Pre, respectively.

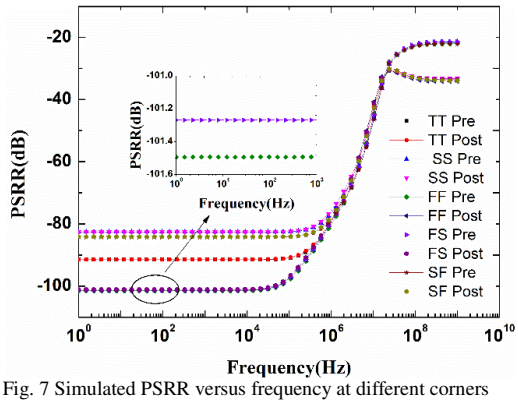


Fig. 7 Simulated PSRR versus frequency at different corners

The relationship between PSRR andfrequency under different supply voltages is presented in Fig. 8. We can see that an excellent PSRR is also exhibited at different supply voltages. For the supply voltage of 0.7 V, the simulated PSRR reaches -91.5 dB at 10 KHz. the simulated PSRR can reach -111.2 dB at 10 KHz when the supply voltage is 0.9 V.

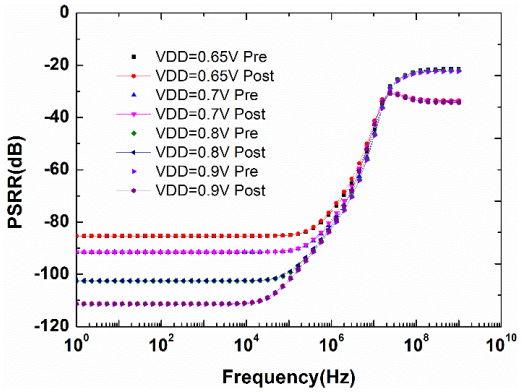


Fig. 8 Simulated PSRR versus frequency at different power supply

The LS is defined as LS= ($\Delta V_{REF}/\Delta V_{DD}$). It can be found from (7) that LS and PSRR are related. When the LS is lower, a high PSRR can be implemented. So using negative feedback, we not only get an excellent PSRR but also obtain a low LS. As shown in Fig. 9, when the simulated supply voltage sweeps from 0.7 V to 1.8 V, the voltage reference only changes 1.9 µV at TT process corner. Consequently, the LS can be calculated to be 0.0017 mV/V.

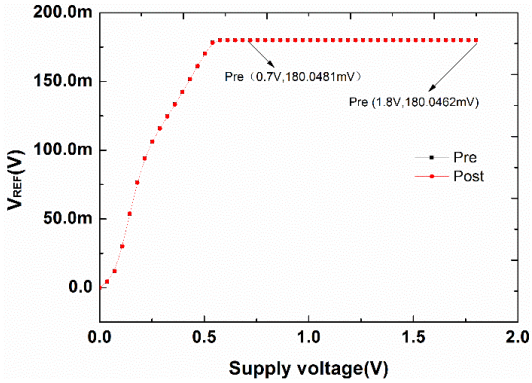


Fig. 9 Simulated Line regulation at different supply voltage.

To guarantee correct function of the circuit against process variation and mismatch, Monte Carlo simulation is performed on 100 samples at room temperature and typical process corner, as shown in Fig. 10. It can be found that the mean value*u* of $V_{REF}$ is 179.69 mV, the standard deviation σ is 3.64 mV. So the coefficient of variation (σ/u) is about 2.0%. By properly setting the size of the transistor and making the current mirrors MP1-MP5 operate in the saturation region, process variations and mismatches can be diminished.

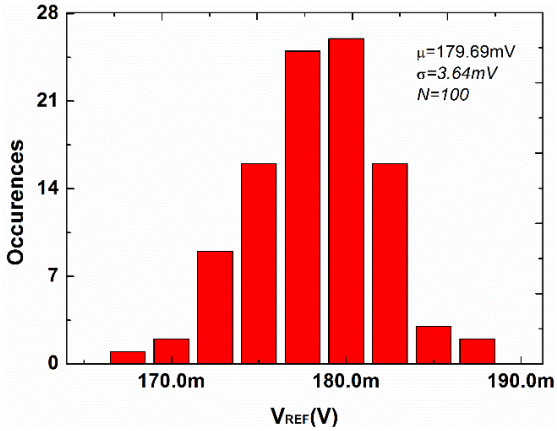


Fig. 10 Monte-Carlo Simulation result of reference voltage

The overall performance is compared between the proposed voltage reference and other voltage references. The results are showed in Table 1. The proposed circuit, Ref [10] and Ref [14] are based on simulation results, while Ref [9] is the measurement result. It can be noticed that the proposedreference has an excellent PSRR and low LS due to the negative feedback technique. Owing to no special device, voltage reference in this paper has a wider application.

## IV. CONCLUSIONS

A 0.7 V 0.0017 mV/V CMOS voltage reference without amplifier is designed in the standard 0.18 µm CMOS process. Low LS and high PSRR are achieved by using negative feedback technique. At $V_{DD}$ = 0.7 V, the simulated PSRR up to -91.5 dB at 10 KHz. Most of transistors operate in the subthreshold region, which reduce supply voltage and power consumption. Through body-bias technique, the TC of the reference voltage is improved. The proposed low-supply voltage high-PSRR low-LR voltage reference can be attractive in the low-power battery-operated electronic applications.

**Table 1**Comparison to other published voltage reference.

| Parameter | Proposed | Ref[9] | Ref[10] | Ref[14] | Unit |
|---|---|---|---|---|---|
| Year | 2018 | 2015 | 2017 | 2016 | |
| CMOS Technology | 0.18µm | 0.18µm | 0.18µm | 0.18µm | - |
| Supply voltage | 0.7 | 0.45 | 0.6 | 0.75 | V |
| $V_{REF}$ | 180 | 118.46 | 441 | 469 | mV |
| Temperature Coefficient | 52 | 63.6 | 25 | 18 | ppm/□ |
| Temperature range | -40-130 | -40-125 | -20-80 | -40-125 | □ |
| σ/µ (Monte Carlo) | 2.0 | 0.6 | 6.6 | 2.2 | - |
| PSRR | -91.5 | -44.2 | -44 | -67 | dB |
| Line regulation | 0.0017 | 1.2 | 30 | 0.14 | mV/V |
| Area | 0.0067 | 0.012 | 0.0071 | 0.0053 | $mm^2$ |
| Verification methods | Simulation | Experimental | Simulation | Simulation | |

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