THRESHOLD VOLTAGE VARIANCE BORROW SAVE ADDER FOR LOW POWER APPLICATIONS

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ABSTRACT: BSA is well known that reduced logic depth allows for operation at low voltages, therefore reducing power dissipation. However, such circuits are particularly susceptible to variations, which may compromise expected benefits. This brief presents a solution for low-power addition under variability, which successfully handles the challenge of increased threshold voltage variation. Specifically, we quantitatively compare the impact of variation on the performance of ripple-carry adder (RCA) and borrow-save adder (BSA), quantify the average power reduction achieved by BSA attained at low voltage values, at the cost of increased delay variation, and propose a technique that enhances BSA tolerance to variations. Using statistical timing evaluation at the 45-nm and 32-nm nodes, we estimate the maximum critical path delay variation and average power dissipation of BSA at different supply voltages. Our analysis reveals that BSA achieves three times smaller standard deviation of maximum delay than RCA at the same supply voltage. In addition, we show that it is possible to substantially reduce the supply voltage, decreasing by almost 60% the overall power dissipation of BSA in comparison to a counterpart operating at nominal voltage while keeping maximum delay less than that of RCA. Furthermore, simple design optimizations in the design of BSA are introduced that trade latency for variability, significantly reducing normalized standard deviation of the maximum delay.

KEYWORDS: Borrow Save Adder(BSA), Ripple Carry Adder(RCA)

INTRODUCTION: significant delay uncertainties have arisen in the deep sub-micron IC design so that the adoption of statistical tools for Timing Analysis has become indispensable, as traditional methods for modeling electrical parameters render inefficient [1]. The fundamental atomic-level randomness encountered in modern semiconductor devices, coupled with difficulties in controlling manufacturing processes precisely, accounts for the fact that manufactured ICs present characteristics that dramatically differ from their initial specifications. In view of these challenges, the pronounced limitations of DeterministicStatic Timing Analysis tools drive both academia and industry to seek efficient solutions considering multiple corner cases, which specify delay characteristics in extreme process and environmental conditions. In this context, Statistical TimingAnalysis emerges as a viable solution. The complexity and increased number of stages involved in the manufacturing process make physical parameters prone to variations. When modeled statistically, parameters are distinguished into inter- and intra-die variations. The former, also termed as die-to-die, are due to mechanisms either in the manufacturing process or because of environmental factors, which cause global shifts, the same across a die, wafer or lot, and the latter, known also as within-die, model device parameters with different variations across a die. Although the contribution of intra-die variations on parameters was negligible in manufacturing process generations of long-channel devices, these variations are taken into account for contemporary digital designs in which low supply voltage values are used [4]. Extensive literature focuses on the modeling of delay uncertainty of simple structures due to environmental and manufacturing process variations. Alioto and Palumbo [5] derive an analytical model that describes the delay sensitivity of a Ripple-Carry Adder composed by Dual-Rail Domino or Mirror Full Adder cells. A model that describes the propagation delay variance of a CMOS inverter is presented in [6], taking into account within-die variations of threshold voltage and the value of input slew, showing that the propagation delay variance is proportional to threshold voltage variance. A great research effort has been focused on the evaluation of a range ofFull Adder topologies (at the transistor level) or of Ripple- Carry topologies in terms of Power and Energy/Power Delay Product. Certain CMOS Full Adder architectures are investigated in from a delay variation perspective, and the noise tolerance of CNFET technology on process variations is explored in. Dorostiet al. [11] assess the mean delay and standard

deviation of Adder structures working on sub-threshold operating region and propose the adoption of folded and deeply pipelined architectures to mitigate delay variations.

LITERATURE SURVEY: In this Paper[1], Technique of this paper carry free addition algorithm is used for reviewing high radix signed digit adders. Advantage isReduces power consumption. Disadvantage of this analysis does not apply to FPGA implementations. In this Paper [2], Technique of this paper investigates the impact of inter- and intra-die variations on binary and high-radix adders that adopt the borrow-save encoding. High-radix adders have been employed for the recoding of multipliers and for determining quotient and root digits in iterative division and square-root algorithms. Advantage is Reduces delay. Disadvantage is High area consumption. In this Paper [3], Technique of this brief analyzes the latency, energy consumption, and effects of process variation on different structures with respect to the design structure and logic depth to propose architectures with higher throughput, lower energy consumption, and smaller performance loss caused by process variation in application specific integrated circuit design. Advantage is reducing sensitivity to process variations. Disadvantage is it has some timing fluctuations. In this Paper [4], Technique of this project, a number of novel 1-bit full adder cells using carbon nanotube field-effect transistor devices are presented. First of all, some two-input XOR/XNOR circuits are proposed, and then, they are employed to form 1-bit full adders. Totally, five full adders with driving power and one without driving power are proposed in this paper, each of which has its own merits. Advantage isrobust against high amplitude of noises. Disadvantage is Delay is high. In this Paper [5], Technique of this brief, we propose a novel and effective splitting based variation reduction technique for gates. We developed a new tool called Timing Uncertainty Reduction by Gate Splitting (TURGS), which reduces the timing variations of a circuit and presents little delay overhead at the primary output. Advantage isReduces timing variations and overhead**.** Disadvantage is High power consumption.

Technique of this Paper [5], presents the comparison of MOSFET and CNTFET devices. we have analyzed and justify why CNTFET is to be a post-CMOS device. For that we have analyzed the quantum capacitance and found that in CNTFET device it

decreases with decrease in oxide thickness whereas in MOSFET device it increases, which leads to performance degradation of the device. Advantage is Reduces leakage power. Disadvantage is Memory overhead. Technique of this paper [7], a novel design technique for ternary logic gates based on CNTFETs is proposed and compared with the existing resistive-load CNTFET logic gate designs. Especially, the proposed ternary logic gate design technique combined with the conventional binary logic gate design technique provides an excellent speed and power consumption characteristics in datapath circuit such as full adder and multiplier. Advantage is Less delay. Disadvantage is Increases leakage power. Technique of this paper [8], a hybrid 1-bit full adder design employing both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic is reported. The design was first implemented for 1 bit and then extended for 32 bit also. Advantage is Significant improvement in terms of power and speed. Disadvantage is Increased carry propagation delay. Technique of this paper [9], presents a comparative study of highspeed, low-power and low voltage full adder circuits. Our approach is based on XOR-XNOR (4T) design full adder circuits combined in a single unit. This technique helps in reducing the power consumption and the propagation delay while maintaining low complexity of logic design. Advantage is the noise performance of the design is superior to other reference. Disadvantage is High memory overhead.Technique of this paper [10], the utilization of Residue Number System (RNS) is investigated as a tool for variation-tolerant design. In particular circuits using various RNS bases are compared in terms of their sensitivity to the variation of process parameters. Advantage is Reduces noise and error. Disadvantage isProvides some critical path delay.

PROPOSED SYSTEM: Luigi Dadda, the computer scientist has invented the DADDA hardware multiplier during 1965. DADDA multiplier is extracted form of parallel multiplier [5]. It is slightly faster and requires fewer gates. Different types of schemes are used in parallel multiplier. The DADDA scheme is one of the parallel multiplier schemes that essentially minimize the number of adder stages required to perform the summation of partial products. This is achieved by using full and half adders to reduce the number of

rows in the matrix number of bits at each summation stage. Even though the DADDA multiplication has regular and less complex structure, the process is slower in manner due to serial multiplication process. Further, DADDA multiplier is less expensive compared to that of Wallace tree multiplier. Hence, in this paper, DADDA multiplier is designed and analysed by considering different methods using full adders involving different logic styles. The algorithm of DADDA multiplier is based on the below matrix form shown in Fig.1. The partial product matrix is formed in the first stage by AND stages which is illustrated in Fig. 2.

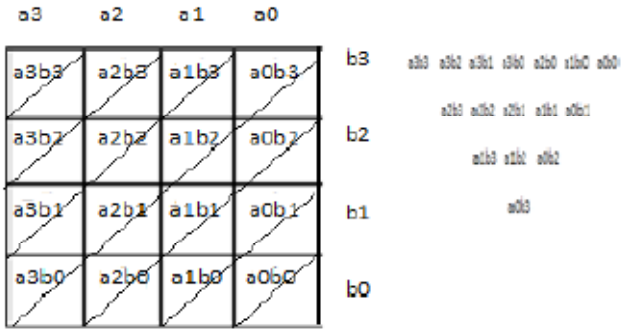

Figure: 4x4 DADDA Multiplier

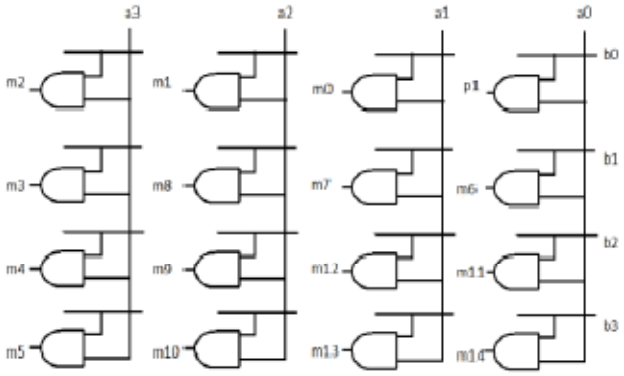

Figure: Product terms generated by a collection of AND gates

Steps involved in DADDA multipliers Algorithm:

- Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding N results.

- Depending on position of the multiplied bits, the wires carry different weights. Reduce the number of partial products to two layers of full adders.
- Group the wires in two numbers, and add them with a conventional adder.

Ripple Carry Adder is the method used to add more number of additions to be performed with the carry in sand carry outs that is to be chained. Thus multiple adders are used in ripple carry adder. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder.

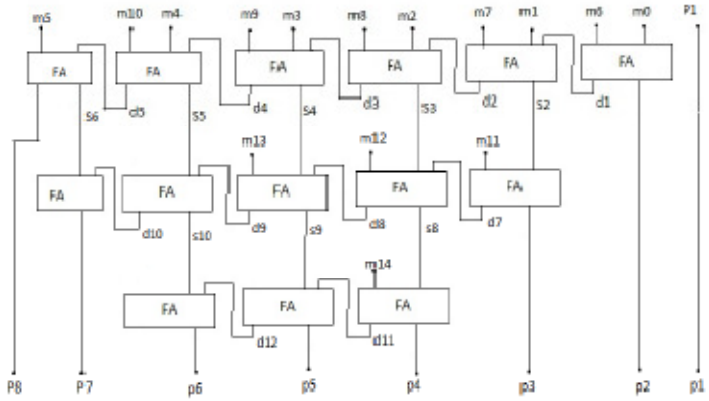

Figure: 4x4 DADDA Multiplier using RCA

Full adder in DADDA multiplier is designed using SR-PL and DPL logic family for better performance. The proposed architecture of DADDA multiplier algorithm using RCA is shown in Fig.3. Steps involved in 4x4 DADDA multiplier using RCA are discussed below. Take any 3 wires with the same weights and give them as input into a full adder. The result will be an output wire of the same weight. Partial product obtained after multiplication is taken at the first stage. The data's are taken with 3 wires and added using adders and the carry of each stage is added with next two data's in the same stage. Partial products reduced to two layers of full adders with same procedure. At the final

stage, same method of ripple carry adder method is performed and thus product terms p1 to p8 is obtained. Carry save adder is the technique used to add more number of additions to be performed with the carry ins and carry outs parallel after generating the partial products, grouped three rows as stage1 and perform addition using carry save method. The proposed architecture of 4x4 bit DADDA multiplier algorithm using CSA is illustrated in Fig: 4

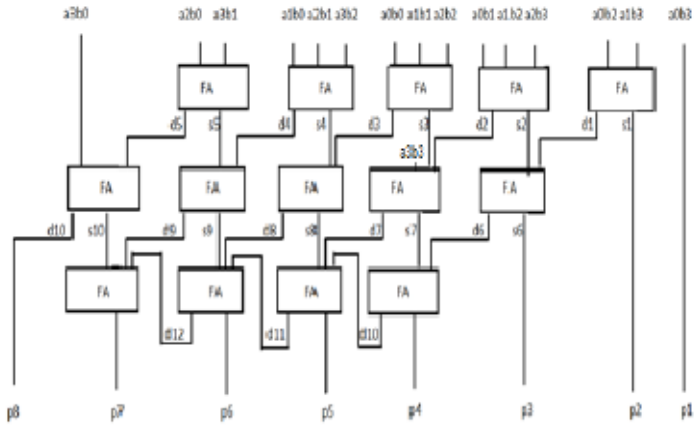

Figure: DADDA Multiplier using CSA

Steps involved in 4x4 DADDA multiplier using CSA are discussed below Take any 3 wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each 3 input wires. Partial product obtained after multiplication is taken at the first stage. The data's are taken with 3 wires and added using full adders and the carry of each stage is saved and send to the next stage. In the second step, the partial products are added with previous stage outputs. At the final stage, the fast adding method namely ripple carry adder [12] is used to reduce the number of stage thus product terms p1 to p8 is performed.

RESULT: The results depicted that the proposed CSLA has higher speed when compared to regular and modified CSLA. compares the mulitiplier circuit for area comparison. When compared to regular and modified CSLA the proposed circuit

occupies less area. In addition to realization of higher speed and lesser area as discussed above, depicted that the proposed architecture consumes less power when compared to the regular and modified CSLA. The proposed CSLA overweighs both the regular and modified CSLA in terms of area, delay and power.

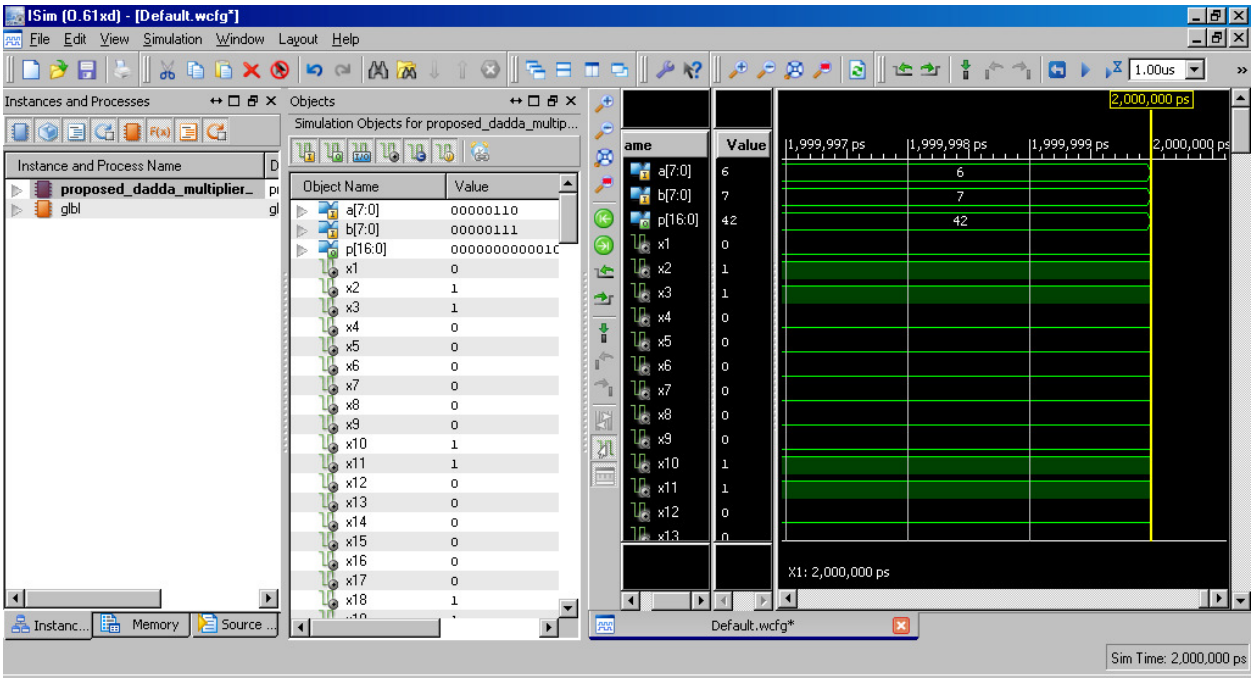

Figure: Simulation Output

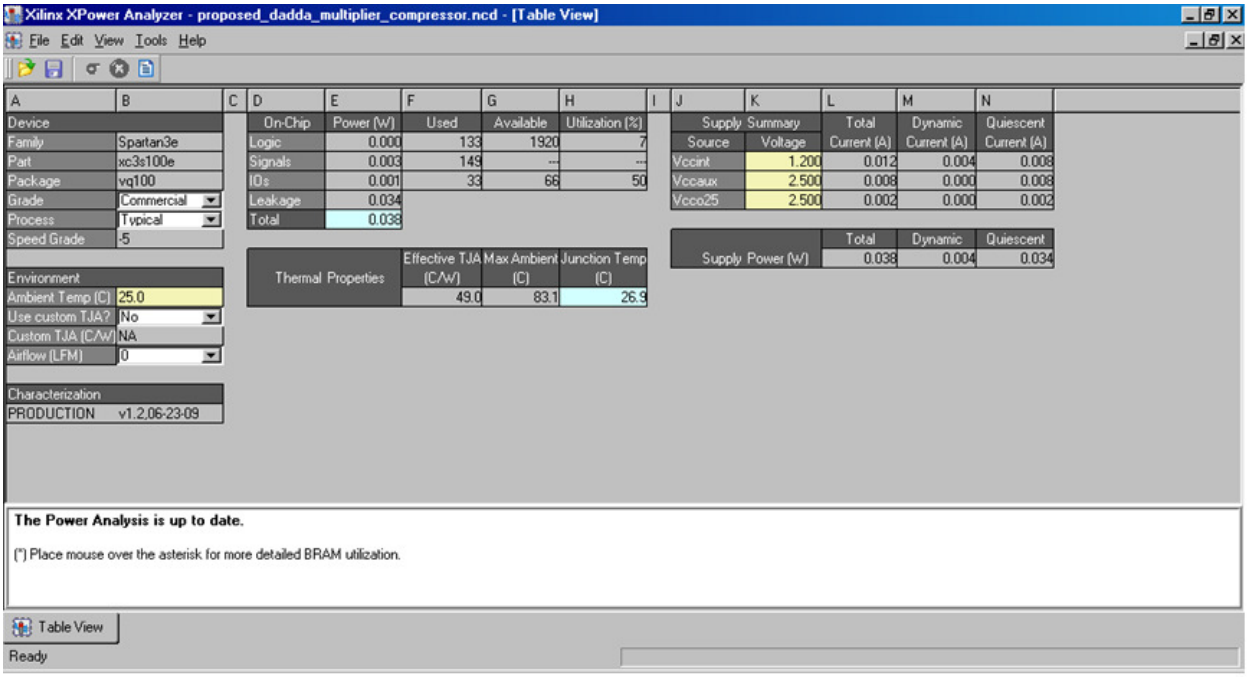

Figure: Power Analysis of DADDA Mulitiplier

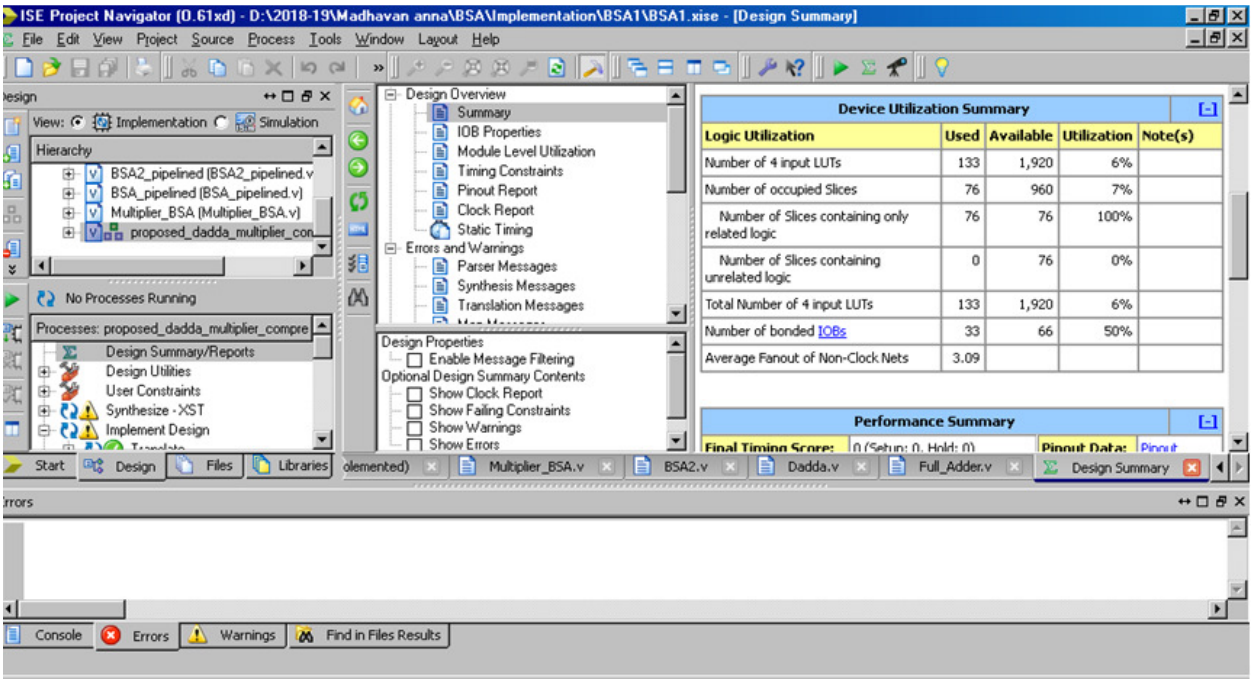

Figure: Area of DADDA Multiplier

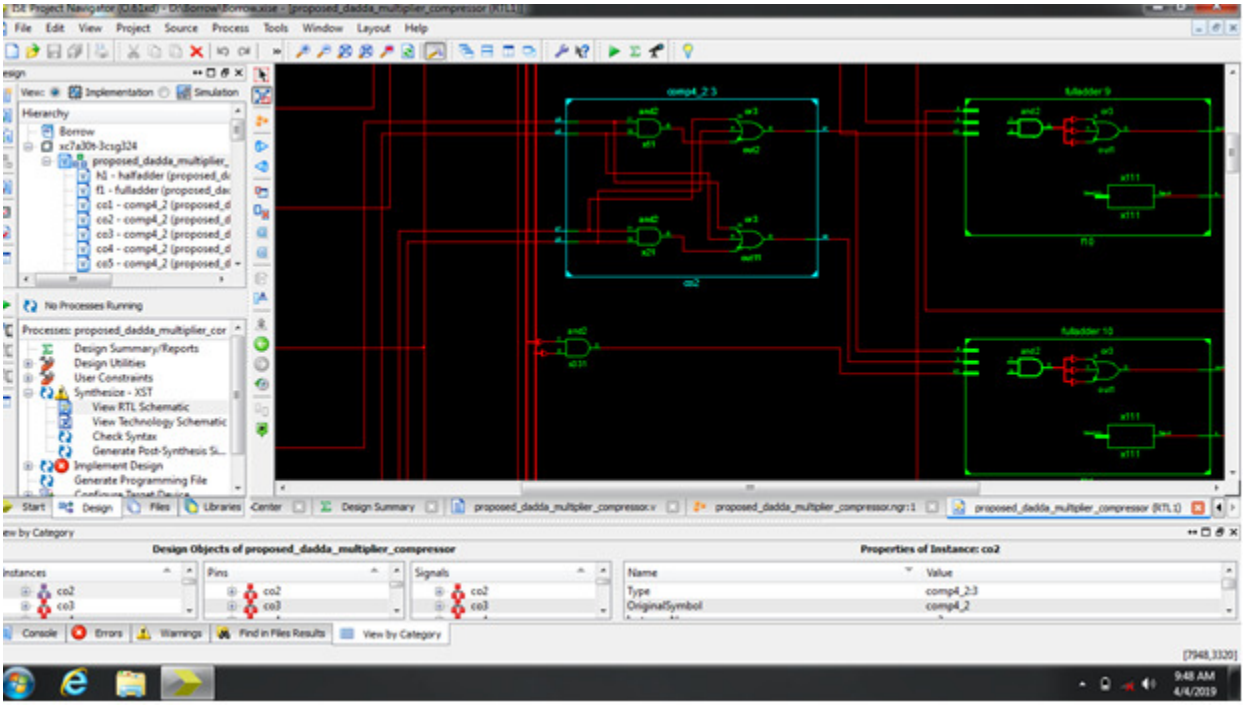

Figure: RTL Schematic Diagram

CONCLUSION: We comparatively examine the effect of threshold voltage variability on the timing behavior of RCAs and BSAs. By modeling the behavior of threshold voltage under fluctuations and using BSIM 4 SPICE models, we estimate the standard deviation of maximum delay for the two aforementioned architectures. The evaluation shows that BSA achieves smaller delay variation than RCA at nominal supply voltage. Furthermore, it is possible to reduce the supply voltage of BSA, attaining the delay constraints imposed by the delay characteristics of RCA, as well as reducing significantly both power dissipation and PDP. The power reduction benefits are validated for both 32-nm and 45-nm technology nodes. Finally, simple introduced interconnection modifications lead to a reduced normalized and non-normalized delay variation for BSA.

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